JSS Mahavidyapeetha

Sri Jayachamarajendra College of Engineering

Department of Electronics & Communication

**LESSON PLAN**

Teacher : **Halesh M. R**  Semester Starting on: **08.03.2021**

Class & Section : **VI semester E&C ‘A & B’ Section** Semester Ending on: **26.06.2021**

Subject with Code: **CMOS VLSI Circuits– EC630**

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| **Session Nos.** | **Topics to be covered** | **Reference** |
| 1 | **Introduction to the subject and brief about COs** | **----** |
| 2 | **Unit 1:** Introduction to VLSI – A Brief History | **Book. 1:** Chapter 1 |
| 3 | MOS Transistors | **Book. 1:** 1.3 |
| 4 | CMOS Logic | **Book. 1:** 1.4 |
| 5 | CMOS fabrication and Layout | **Book. 1:** 1.5 |
| 6 | VLSI Design Flow | **Book. 1:** 1.6 |
| 7 | VLSI Fabrication | **Book. 1:** 1.7 |
| 8 | Packaging, and testing | **Book. 1:** 1.7 |
| 9 | **Unit 2:** MOS Transistor Theory | **Book. 1:** Chapter 2 |
| 10 | Ideal I-V Characteristics | **Book. 1:** 2.2 |
| 11 | Ideal I-V Characteristics continued.. | ----‘’---- |
| 12 | C-V Characteristics | **Book. 1:** 2.3 |
| 13 | Non ideal I-V Effects | **Book. 1:** 2.4 |
| 14 | Non ideal I-V Effects continued | ----‘’---- |
| 15 | DC Transfer Characteristics | **Book. 1:** 2.5 |
| 16 | Switch - level RC Delay Models | **Book. 1:** 2.6 |
| 17 | **Unit 3:** Circuit Characterization Introduction | **Book. 1:** Chapter 4 |
| 18 | Performance Estimation Introduction | **Book. 1:** 4.1 |
| 19 | Delay Estimation | **Book. 1:** 4.2 |
| 20 | Logical effort and transistor sizing | **Book. 1:** 4.3 |
| 21 | Power Dissipation | **Book. 1:** 4.4 |
| 22 | Interconnect | **Book. 1:** 4.5 |
| 23 | Design Margin | **Book. 1:** 4.6 |
| 24 | Reliability | **Book. 1:** 4.7 |
| 25 | **Unit 4:** Combinational and Sequential circuit design | **Book. 4:** Chap. 7 & 8 |
| 26 | Combinational MOS Logic Circuits | **Book. 4:** Chapter 7.3 |
| 27 | Complex Logic Circuits | **Book. 4:** Chapter 7.4 |
| 28 | Sequential MOS Logic Circuits - SR Latch Circuit | **Book. 4:** Chapter 8.3 |
| 29 | Clocked Latch and Flip-Flop Circuits | **Book. 4:** Chapter 8.4 |
| 30 | Clocked Latch and Flip-Flop Circuits continue. | ----‘’---- |
| 31 | CMOS D-Latch and Edge-Triggered Flip-Flop | **Book. 4:** Chapter 8.5 |
| 32 | CMOS D-Latch and Edge-Triggered Flip-Flop continue. | ----‘’---- |
| 33 | **Unit 5: Dynamic Logic Circuits** | **Book. 4:** Chapter 9 |
| 34 | Voltage Bootstrapping | **Book. 4:** Chapter 9.3 |
| 35 | Synchronous Dynamic Circuit Techniques | **Book. 4:** Chapter 9.4 |
| 36 | High-Performance Dynamic CMOS Circuits | **Book. 4:** Chapter 9.5 |
| 37 | Semiconductor Memories | **Book. 4:** Chapter 10 |
| 38 | Read-Only Memory (ROM) Circuits | **Book. 4:** Chapter 10.2 |
| 39 | Static Read-Write Memory (SRAM) Circuits | **Book. 4:** Chapter 10.3 |
| 40 | Dynamic Read-Write Memory (DRAM) Circuits | **Book. 4:** Chapter 10.4 |

Signature of Teacher Signature of HOD/Chair Person